CLAIMS

What is claimed is:

1. A method for reducing interrupts while tracing an application in a data processing system, the method comprising:

receiving at a tracing function an indication that at least a portion of executable code from an application has been loaded into a memory block prior to execution of the portion of executable code; and

altering by the tracing function at least one operating-system-defined memory access protection parameter to allow read access to the memory block.

2. The method of claim 1 wherein the receiving step and the altering step are performed for each memory fault for the application.

3. The method of claim 2 wherein a memory fault includes a page fault or a segment fault.

4. An apparatus for reducing interrupts while tracing an application in a data processing system, the apparatus comprising:

means for receiving at a tracing function an indication that at least a portion of executable code from an application has been loaded into a memory block prior to execution of the portion of executable code; and

means for altering by the tracing function at least one operating-system-defined memory access protection parameter to allow read access to the memory block.

5. The apparatus of claim 4 wherein the receiving means and the altering means are activated for each memory fault for the application.

6. The method of claim 5 wherein a memory fault includes a page fault or a segment fault.

7. A computer program product in a computer-readable medium for use in a data processing system for reducing interrupts while tracing an application, the computer program product comprising:

instructions for receiving at a tracing function an indication that at least a portion of executable code from an application has been loaded into a memory block prior to execution of the portion of executable code; and

instructions for altering by the tracing function at least one operating-system-defined memory access protection parameter to allow read access to the memory block.

8. The computer program product of claim 7 wherein the receiving means and the altering means are activated for each memory fault for the application.

9. The computer program product of claim 8 wherein a memory fault includes a page fault or a segment fault.

10. A method for reducing interrupts while tracing an application in a data processing system, the method comprising:

initiating execution of tracing software;

allocating a data output buffer in physical memory, wherein the data output buffer holds output data from the tracing software; and

writing output data to the data output buffer by the tracing software using physical memory addressing.

11. A method for reducing interrupts while tracing an application in a data processing system, the method comprising:

initiating execution of tracing software;

allocating a data output buffer, wherein the data output buffer holds output data from the tracing software; and

configuring a translation register in a processor of the data processing system for the data output buffer.

12. An apparatus for reducing interrupts while tracing an application in a data processing system, the apparatus comprising:

means for initiating execution of tracing software, wherein a data output buffer holds output data from the tracing software; and

means for writing output data to the data output buffer by the tracing software using physical memory addressing.

13. An apparatus for reducing interrupts while tracing an application in a data processing system, the apparatus comprising:

means for initiating execution of tracing software, wherein a data output buffer holds output data from the tracing software; and

means for configuring a translation register in a processor of the data processing system for the data output buffer.

14. A computer program product in a computer-readable medium for use in a data processing system for reducing interrupts while tracing an application, the computer program product comprising:

instructions for initiating execution of tracing software, wherein a data output buffer holds output data from the tracing software; and

instructions for writing output data to the data output buffer by the tracing software using physical memory addressing.

15. A computer program product in a computer-readable medium for use in a data processing system for reducing interrupts while tracing an application, the computer program product comprising:

instructions for initiating execution of tracing software, wherein a data output buffer holds output data from the tracing software; and

instructions for configuring a translation register in a processor of the data processing system for the data output buffer.

16. A method for reducing interrupts while tracing an application in a data processing system, the method comprising:

receiving an indication of an instruction to be traced, wherein the instruction is associated with an instruction address;

in response to receiving the indication of the instruction to be traced, retrieving the instruction address;

writing the instruction address to a trace output buffer in memory; and

writing instruction resolution information to a trace output buffer, wherein the instruction resolution information comprises operating-system-defined memory allocation information or generated application code.

17. The method of claim 16 further comprising:

receiving an indication of a change to memory allocation information for an application, wherein the step of writing operating-system-defined memory allocation information is performed in response to receiving the indication of the change to memory allocation information for the application.

18. The method of claim 16 further comprising:

reconciling the instruction address with the operating-system-defined memory allocation information to determine a location of the instruction in an application file or module.

19. The method of claim 16 further comprising:

retrieving a copy of the instruction from an application file or module in relation to the instruction address.

20. The method of claim 16 further comprising:

reconciling the instruction address with the generated application code to determine a location of the instruction within the generated application code.

21. The method of claim 16 further comprising:

retrieving a copy of the instruction from the generated application code in relation to the instruction address.

22. An apparatus for reducing interrupts while tracing an application in a data processing system, the apparatus comprising:

means for receiving an indication of an instruction to be traced, wherein the instruction is associated with an instruction address;

means for retrieving the instruction address in response to receiving the indication of the instruction to be traced;

means for writing the instruction address to a trace output buffer in memory; and

means for writing instruction resolution information to a trace output buffer, wherein the instruction resolution information comprises operating-system-defined memory allocation information or generated application code.

23. The apparatus of claim 22 further comprising:

means for receiving an indication of a change to memory allocation information for an application, wherein the step of writing operating-system-defined memory allocation information is performed in response to receiving the indication of the change to memory allocation information for the application.

24. The apparatus of claim 22 further comprising:

means for reconciling the instruction address with the operating-system-defined memory allocation information to determine a location of the instruction in an application file or module.

25. The apparatus of claim 22 further comprising:

means for retrieving a copy of the instruction from an application file or module in relation to the instruction address.

26. The apparatus of claim 22 further comprising:

means for reconciling the instruction address with the generated application code to determine a location of the instruction within the generated application code.

27. The apparatus of claim 22 further comprising:

means for retrieving a copy of the instruction from the generated application code in relation to the instruction address.

28. A computer program product in a computer-readable medium for use in a data processing system for reducing interrupts while tracing an application, the computer program product comprising:

means for receiving an indication of an instruction to be traced, wherein the instruction is associated with an instruction address;

means for retrieving the instruction address in response to receiving the indication of the instruction to be traced;

means for writing the instruction address to a trace output buffer in memory; and

means for writing instruction resolution information to a trace output buffer, wherein the instruction resolution information comprises operating-system-defined memory allocation information or generated application code.

29. The computer program product of claim 28 further comprising:

means for receiving an indication of a change to memory allocation information for an application, wherein the step of writing operating-system-defined memory allocation information is performed in response to receiving the indication of the change to memory allocation information for the application.

30. The computer program product of claim 28 further comprising:

means for reconciling the instruction address with the operating-system-defined memory allocation information to determine a location of the instruction in an application file or module.

31. The computer program product of claim 28 further comprising:

means for retrieving a copy of the instruction from an application file or module in relation to the instruction address.

32. The computer program product of claim 28 further comprising:

means for reconciling the instruction address with the generated application code to determine a location of the instruction within the generated application code.

33. The computer program product of claim 28 further comprising:

means for retrieving a copy of the instruction from the generated application code in relation to the instruction address.

34. A method for reducing interrupts while tracing an application in a data processing system, the method comprising:

receiving an indication of an instruction to be traced, wherein the instruction is associated with an instruction address;

storing the instruction address;

getting a previously stored instruction address;

retrieving a previously executed instruction using the previously stored instruction address; and

writing the retrieved instruction to a trace output buffer.

35. The method of claim 34 wherein a processor in the data processing system supports variable length instructions.

36. The method of claim 34 further comprising:

retrieving a branch-from address; and

retrieving a set of previously executed instructions using the previously stored instruction address and the branch-from address.

37. An apparatus for reducing interrupts while tracing an application in a data processing system, the apparatus comprising:

means for receiving an indication of an instruction to be traced, wherein the instruction is associated with an instruction address;

means for storing the instruction address;

means for getting a previously stored instruction address;

means for retrieving a previously executed instruction using the previously stored instruction address; and

means for writing the retrieved instruction to a trace output buffer.

38. The apparatus of claim 37 wherein a processor in the data processing system supports variable length instructions.

39. The apparatus of claim 37 further comprising:

means for retrieving a branch-from address; and

means for retrieving a set of previously executed instructions using the previously stored instruction address and the branch-from address.

40. A computer program product in a computer-readable medium for use in a data processing system for reducing interrupts while tracing an application, the computer program product comprising:

instructions for receiving an indication of an instruction to be traced, wherein the instruction is associated with an instruction address;

instructions for storing the instruction address;

instructions for getting a previously stored instruction address;

instructions for retrieving a previously executed instruction using the previously stored instruction address; and

instructions for writing the retrieved instruction to a trace output buffer.

41. The computer program product of claim 40 wherein a processor in the data processing system supports variable length instructions.

42. The computer program product of claim 40 further comprising:

instructions for retrieving a branch-from address; and

instructions for retrieving a set of previously executed instructions using the previously stored instruction address and the branch-from address.